REMARKS

Claims 1-22 remain pending in the current Application. No amendments to the claims are being made herein.

Provisional Nonstatutory Obviousness-Type Double Patenting Rejection

Applicant respectfully submits that claims 1-22 are patentably distinct over Application No. 10/657,797. For example, the Examiner states that the claims are not patentably distinct because "although the copending claim 1 does not recite the transfer between the memory and at least two registers as claimed, it would have been obvious to one of ordinary skill in the art to transfer between the memory and two registers as claimed because the copending claim 1 also taught a transfer between the memory and at least one register." However, claim 1 of the current Application isn't simply claiming a transfer between memory and at least two registers, but specifically claims that the at least one or more instructions specifies *a number of register elements* to be transferred between *each* of the at least two of the plurality of general purpose registers and the memory, which is not even addressed or suggested by copending claim 1 and is not at all obvious over copending claim 1. Therefore, the use of "at least one register" in copending claim 1 does not render obvious specifying the particular number of register elements per each of at least two registers as claimed in claim 1 of the current Application.

Applicant also respectfully submits that claims 1-22 are patentably distinct over Application No. 10.657,510. For example, the Examiner state the claims are not patentably distinct because "although the copending claim 1 did not recite the number of data elements to tbe transferred as claimed, it would have been obvious to one of ordinary skill in the art to include the number of data elements to be transferred because the copending claim 1 also taught the determination of the data element size in a register." However, again, current claim 1 does not simply claim providing a total number of data elements to be transferred, but specifies *a number of register elements* to be transferred between *each* of the at least two of the plurality of general purpose registers and the memory. In copending claim 1, although the size is provided, this does not suggest providing an instruction which specifies a number or register elements to be transferred between each of at least two registers. Therefore, the size of a data element as in

copending claim 1 does not render obvious specifying the particular number of register elements per each of at least two registers as claimed in claim 1 of the current Application.

Therefore, Applicants respectfully request that the Examiner withdraw the provisional rejection of obviousness-type double patenting.

Rejection of claims 1-16 under 35 U.S.C. 102(b)

Applicant respectfully submits that claims 1-16 are patentable over US Patent No. 5,870,596 (hereinafter referred to as Yoshida) because Yoshida does not teach or suggest each an every element, as required in a finding of anticipation.

With respect to claims 1, 5, and 15, each of claims 1, 5, and 15 includes at least one or more instruction specifying a number of register elements to be transferred between ***each*** of the at least two of the plurality of general purpose registers and the memory. That is, the number of register elements specified corresponds to the number of register elements transferred between each register of the at least two registers and memory. Therefore, the number of register elements refers to a number of register elements within a particular general purpose register. Yoshida at least does not teach or suggest the number of register elements as claimed. The Examiner cites that col. 24, lines 14-21, which describes the loading of 4 bytes according to internal code LDM1 to R1, and col. 24, lines 45-50 which describes the loading of 4 bytes into registers R4 according to internal code LDM2. However, note that the number of elements loaded into each registers (R1 and R2) is always 4. That is, there is no field or specifier provided in the LDM instruction to specify this number. For example, as described in col. 10, lines 10-11 and lines 22-23 with respect to the LDM and STM instructions, the data transferred to and from each of the registers is respectively 4 bytes. Therefore, any number of registers can be specified in which to load from or store to, but the data transferred is always 4 bytes. Therefore, there is no teaching or suggestion of specifying a number of register elements, as claimed. Furthermore, one would not be motivated to do so, since the data transferred in Yoshida is fixed to 4 bytes. Therefore, for at least these reasons, Applicant submits claims 1, 5, and 15 are allowable over Yoshida.

With respect to claims 8, 13, and 15, each of claims 8, 13, and 15 includes at least one or more instructions specifying *which* data elements of the at least two of the plurality of general

purpose registers are to be transferred. This is also not taught or suggested by the LDM or STM instructions of Yoshida. That is, there is no field or specifier provided for the LDM or STM to specify which data elements are to be transferred. In addition, Applicant submits that the pertinence of Yoshida with respect to the rejection of independent claims 8, 13, and 15, and their respective dependent claims is not apparent since, for example, claim 8 and 13 include different limitations than claims 1 and 5, and claim 15 includes additional limitations than claim 1. Therefore, the rejection of these claims is not clearly explained as per the requirements outlined in 37 C.F.R. 1.104(c)(2). Applicant respectfully points out to the Examiner, "[a] plurality of claims should never be grouped together in a common rejection, unless the rejection is equally applicable to all claims in the group" (MPEP 707.07(d)).

Claims 2-4, 6, 7, 9-12, 14, and 16 have not been independently addressed since they depend directly or indirectly from allowable claims 1, 5, 8, 13, or 15, and are therefore patentable over Yoshida for at least those reasons provided above with respect to these claims.

Rejection of claims 1-22 under 35 U.S.C. 102(b)

Applicant respectfully submits that claims 1-22 are patentable over US Patent No. 6,170,001 (hereinafter referred to as Hinds) because Hinds does not teach or suggest each an every element, as required in a finding of anticipation.

With respect to claims 1, 5, and 15, each of claims 1, 5, and 15 includes at least one or more instruction specifying a number of register elements to be transferred between ***each*** of the at least two of the plurality of general purpose registers and the memory. That is, the number of register elements specified corresponds to the number of register elements transferred between each register of the at least two registers and memory. Therefore, the number of register elements refers to a number of register elements within a particular general purpose register. Hinds at least does not teach or suggest the number of register elements as claimed. The Examiner cites that col. 2, lines 60-67, which describes the number of odd data words, and col. 10, lines 54-64 which describes the use of a data type bit specifying the use of single or double precision. However, neither the number of odd data words nor the data type bit which simply indicates the use of single or double precision teach or suggest a number of register elements *transferred to/from each register*, as claimed. The Examiner further points to co. 20, lines 11-48

for the detail of operand data elements in a bank of registers, however, no details is provided of an instruction. This section describes operation of the VFPv1 (a floating point system architecture) which provides access to the registers in either scalar or vector mode. However, no instruction specifying the number of registers elements as claimed is discussed. Therefore, for at least these reasons, Applicant submits claims 1, 5, and 15 are allowable over Hinds.

With respect to claims 8, 13, and 15, each of claims 8, 13, and 15 includes at least one or more instructions specifying *which* data elements of the at least two of the plurality of general purpose registers are to be transferred. This is also not taught or suggested by Hinds. That is, neither the odd or even number of data words nor the VFPv1 discussed in col. 20 of Hinds specify which data elements are to be transferred. In addition, Applicant submits that the pertinence of Hinds with respect to the rejection of independent claims 8, 13, and 15, and their respective dependent claims is not apparent since, for example, claim 8 and 13 include different limitations than claims 1 and 5, and claim 15 includes additional limitations than claim 1. Therefore, the rejection of these claims is not clearly explained as per the requirements outlined in 37 C.F.R. 1.104(c)(2). Applicant respectfully points out to the Examiner, "[a] plurality of claims should never be grouped together in a common rejection, unless the rejection is equally applicable to all claims in the group" (MPEP 707.07(d)).

Claims 2-4, 6, 7, 9-12, 14, and 16-22 have not been independently addressed since they depend directly or indirectly from allowable claims 1, 5, 8, 13, or 15, and are therefore patentable over Hinds for at least those reasons provided above with respect to these claims.

Rejection of claims 1, 5, 8, 10, 13, and 15 under 35 U.S.C. 102(b)

Applicant respectfully submits that claims 1, 5, 8, 10, 13, and 15 are patentable over US Patent No. 4,760,545 (hereinafter referred to as Inagami) because Inagami does not teach or suggest each an every element, as required in a finding of anticipation.

With respect to claims 1, 5, and 15, each of claims 1, 5, and 15 includes at least one or more instruction specifying a number of register elements to be transferred between ***each*** of the at least two of the plurality of general purpose registers and the memory. That is, the number of register elements specified corresponds to the number of register elements transferred between each register of the at least two registers and memory. Therefore, the number of register

elements refers to a number of register elements within a particular general purpose register. Inagami at least does not teach or suggest the number of register elements as claimed. The Examiner refers to fig. 4b, stating that "L" is the number of vector elements to be transferred. The Examiner also refers to col. 6, lines 52-68 as providing the number specified by instruction. However, although L specifies a number of vector elements, the value L does not specify a number of register elements transferred to/from *each register of at least two registers* as claimed. Therefore, for at least these reasons, Applicant submits claims 1, 5, and 15 are allowable over Inagami.

With respect to claims 8, 13, and 15, each of claims 8, 13, and 15 includes at least one or more instructions specifying *which* data elements of the *at least two of the plurality of general purpose registers* are to be transferred. This is also not taught or suggested by Inagami. That is, fig. 4b does not include a field which indicates which data elements of at least two registers are to be transferred. At most, D1 indicates a start element for a particular vector register R1, but does not specify which data elements of the at least two of the plurality of general purpose registers are to be transferred, as claimed. In addition, Applicant submits that the pertinence of Inagami with respect to the rejection of independent claims 8, 13, and 15, and their respective dependent claims is not apparent since, for example, claim 8 and 13 include different limitations than claims 1 and 5, and claim 15 includes additional limitations than claim 1. Therefore, the rejection of these claims is not clearly explained as per the requirements outlined in 37 C.F.R. 1.104(c)(2). Applicant respectfully points out to the Examiner, "[a] plurality of claims should never be grouped together in a common rejection, unless the rejection is equally applicable to all claims in the group" (MPEP 707.07(d)).

Claims 2-4, 6, 7, 9-12, 14, and 16-22 have not been independently addressed since they depend directly or indirectly from allowable claims 1, 5, 8, 13, or 15, and are therefore patentable over Inagami for at least those reasons provided above with respect to these claims.

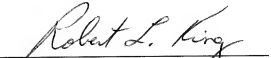
Conclusion

The Office Action contains numerous statements characterizing the claims, the Specification, and the prior art. Regardless of whether such statements are addressed by Applicants, Applicants refuse to subscribe to any of these statements, unless expressly indicated by Applicants.

Applicants respectfully solicit allowance of the pending claims. Contact me if there are any issues regarding this communication or the current Application.

If Applicant has overlooked any additional fees, or if any overpayment has been made, the Commissioner is hereby authorized to credit or debit Deposit Account 503079, Freescale Semiconductor, Inc.

Respectfully submitted,

By: 

Robert L. King
Attorney of Record
Reg. No.: 30,185
Telephone: (512) 996-6839
Fax No.: (512) 996-6854

SEND CORRESPONDENCE TO:

Freescale Semiconductor, Inc.
Law Department

Customer Number: 23125